REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 and 2 remain in this case. Claims 1 and 2 are amended.

The specification is amended, in the first paragraph on the first page, to reflect the serial number of the related application, as requested by the Examiner. No new matter is presented.

The undersigned notes the indication that the priority document has not yet been received. On information and belief, the undersigned understands that a certified copy of the priority document is on order, and that it will be provided to the Patent and Trademark Office promptly upon its receipt.

The undersigned notes the requirement for a new executed Declaration. On information and belief, the undersigned understands that the inventors have been contacted to execute a substitute declaration, and that it will be provided to the Patent and Trademark Office promptly once the executed declaration is received.

The undersigned notes the objection to the drawings. We are submitting replacement drawings, with this paper, that correct the figure numbers themselves, as pointed out by the Examiner. Applicants submit that these new drawings overcome the objection.

The provisional obviousness-type double patenting rejections of claims 1 and 2 are noted. Upon allowance of either this case or the copending application S.N. 10/017,777 upon which the rejection is based, and assuming that the double patenting rejection is still appropriate (depending on the claims in the respective applications at that time), Applicants will then consider a terminal disclaimer to obviate the basis of the rejection.

Claims 1 and 2 were rejected under §103 as unpatentable over the Laurenti et al. patent[3] in view of the Guerra et al. reference[4]. The Examiner asserted that the Laurenti et al. patent discloses determining effective addresses of instructions in a program executed on a pipelined architecture with no external visibility into the pipeline, but did not disclose the specific steps of the claim. The Examiner asserted that the Guerra et al. reference teaches those features, specifically "the capability to determine, calculate, compute, and report of instruction delay" as required by claim 1. The Examiner further asserted that one skilled in the art would have obviously combined the teachings of Guerra et al. into the Laurenti et al. disclosure to model and integrate pipelined architecture, as motivated by the abstract of Guerra et al.[5]

Applicants respectfully traverse the §103 rejection of claims 1 and 2, on the grounds that the combined teachings of the applied references fall short of the requirements of claim 1, and that there is no suggestion from the prior art to modify those teachings in such a manner as to reach the claims.

Claims 1 and 2 are both amended to clarify the syntax of the recited method. Applicants submit that the amendment presented to the claims is not presented for reasons of patentability; Applicants further submit that this amendment is in no way narrowing to either claim, in that there is no scope that is covered by original claims 1 and 2 that is not also covered by amended claims 1 and 2, respectively.[6] No new matter is presented by this amendment.

Claim 1 requires, among other steps, the calculating of a current effective address delay of an instruction that is determined to be in the pipeline. The claim further requires determining whether a valid effective address is available for the instruction, based on that current effective address delay, computing the effective address responsive to determining that

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[3] U.S. Patent No. 6,658,578 B1, issued December 2, 2003 to Laurenti et al., and commonly assigned with this application. The European counterpart of this patent was published on April 12, 2000, as European Patent Application Publication No. EP 0992 916 A1, and as such the contents of the European counterpart are available as prior art under §102(b) and §103.

[4] Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", *ACM* (June, 1999), pp. 964-69.

[5] Office Action of October 20, 2004, page 8.

a valid effective address is not available, and then reporting the effective address for the instruction. As described in the specification,[7] the invention of amended claim 1 provides important visibility into instruction effective addresses during software verification, even in those cases for which the effective address is not available because it has been already used or altered.

Accepting for the sake of argument that the Laurenti et al. patent teaches the elements of the preamble, Applicants agree with the Examiner that it fails to disclose the specific steps of the method. But Applicants disagree with the Examiner that the recited steps of claim 1 are disclosed by the Guerra et al. reference. Applicants submit specifically that the Guerra et al. reference nowhere discloses the determining of whether a valid effective address is available for an instruction in a pipeline, much less based on a calculated current effective address delay for the instruction as required by the claim; Applicants further specifically submit that the Guerra et al. reference nowhere discloses the computing of the effective address of an instruction responsive to determining that a valid effective address is not available, also required by the claims.

The cited location of the Guerra et al. reference in fact discloses nothing regarding effective addresses of an instruction, and therefore necessarily discloses nothing regarding determining whether a valid effective address is available, nor regarding the computing of such an address if none is available. Instead, the Guerra et al. reference discloses only that, in the event of an interrupt occurring with a conditional branch in the instruction fetch pipeline stage, the interrupt is delayed by one instruction cycle so that a "delay slot" instruction is executed before the interrupt is serviced, permitting the target address of the branch to be used as the return address from the interrupt routine.[8] There is no determining of any effective address for an instruction disclosed at this location of the reference, and the delaying of a conditional branch instruction nowhere corresponds to such a determining. And there is certainly no

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[6] *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 535 U.S. 722, 62 USPQ2d 1705 (2002), *on remand*, 304 F.3d 1289, 64 USPQ2d 1698 (Fed. Cir. 2002).

[7] *See* specification of S.N. 10/022,972 at page 16, line 14 through page 17, line 18.

[8] Guerra et al., *supra*, page 966, right-hand column, last paragraph.

disclosure of the computing of an effective address of an instruction disclosed at this location of the reference, much less such calculating responsive to determining that a valid effective address is not available (especially considering that no such determining is disclosed by the reference either). Applicants therefore respectfully submit that the combination of the Laurenti et al. and Guerra et al. references necessarily falls short of the requirements of amended claim 1.

Applicants further respectfully submit that there is no suggestion from the prior art, especially from the Laurenti et al. and Guerra et al. references, to modify these alleged combined teachings in such a manner as to reach amended claim 1. Considering that the Laurenti et al. patent is not asserted to disclose the particular method steps, and also considering that the Examiner erroneously equated the statement that "the cache controller will be disabled to guarantee that external program bus slots are always available" with disclosure of the need to determine effective addresses when not available, Applicants submit that the Laurenti et al. patent provides no suggestion to modify its teachings to provide the determining and computing steps of the claim. The Guerra et al. reference also lacks such suggestion, not only considering that it fails to mention anything about effective addresses of instructions, but also because it is directed solely to full system simulation of the operation of a processor in executing application program. In fact, the techniques disclosed in the Guerra et al. reference for developing its simulation model are directed purely to such simulation, and cannot be applied to hardware emulation and software verification using source hardware and target hardware, as can the method of amended claim 1 in this case.

Lacking such suggestion from the references, Applicants respectfully submit that the improper use, in hindsight, of their own teachings is required in order to combine the Laurenti et al. and Guerra et al. references in such a manner as to reach claim 1 in this case. Applicants therefore respectfully traverse the rejection of claims 1 and 2, and submit that amended claims 1 and 2 are in fact patentably distinct over the Laurenti et al. and Guerra et al. references that were applied in the rejection.

The undersigned is somewhat confused by the treatment of claim 2 in the Office Action. On the one hand, the Laurenti et al. and Guerra et al. references are applied against the claim,[9] but on the other hand, the Examiner indicates that "[c]laim 2 (b) and (c)" would be allowable if rewritten in independent form.[10] And the Office Action further concludes that "Claims 1-2" are subject to a "35 USC 103" rejection.[11]

In either case, Applicants respectfully submit that amended claim 2 is patentably distinct over the applied references, for the same reasons as discussed above relative to amended claim 1 upon which it depends. Applicants further respectfully submit that amended claim 2 is further distinct over the references, because there is no disclosure or suggestion from the applied references to regarding the determining of whether a current effective address delay is zero, and performing the computing step responsive to the current effective address delay being less than zero, as required by amended claim 2. As mentioned above, there is no discussion in the references of the determining and computing steps of claim 1; there necessarily can be no such disclosure or suggestion of the determining and computing steps of claim 2, in which actions are taken relative to specific values resulting from those steps.

For these additional reasons, Applicants submit that amended claim 2 is also patentably distinct over the applied references in this case.

The references cited as pertinent, but which were not applied against the claims, have been considered, but are not felt to come within the scope of the claims in this case.

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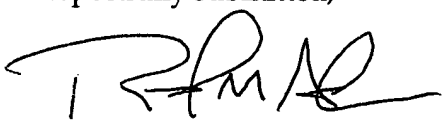
[9] Office Action, *supra,* pages 8 and 9.
[10] *Id.,* at page 9, §14.
[11] *Id.,* at page 9, §15.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of the above-referenced application is therefore respectfully requested.

Respectfully submitted,



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CERTIFICATE OF MAILING

37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on **December 23, 2004.**

Rodney M. Anderson
Registry No. 31,939

Amendment to the Drawings:

The attached replacement sheets 2 through 11,[1] and its corresponding annotated sheets 2 through 11,[2] include changes to Figures 3A, 3B, 4A through 4H, 5A, 5B, and 6A through 6F.

Specifically, the references to the figure numbers themselves are changed to be consistent with the specification, by now placing the alphabetic characters (A through H) in upper case.

[1] Labeled "Replacement Sheet".
[2] Labeled "Annotated Marked-up Drawings".

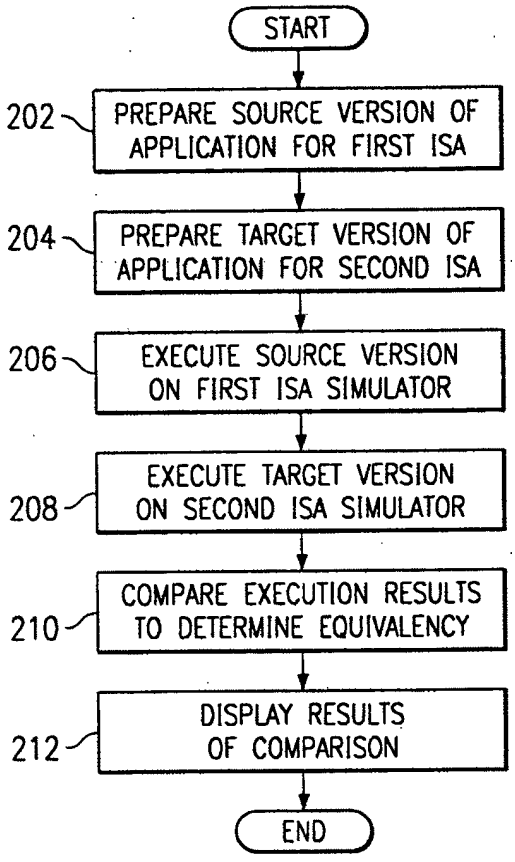

FIG. 2

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
401	STM data1, AR3	EMPTY	402	MOV data1, AR3	EMPTY
	LD #1, A			MOV #1, AC0	
	NOP			NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4a 4A

FIG. 3a 3A

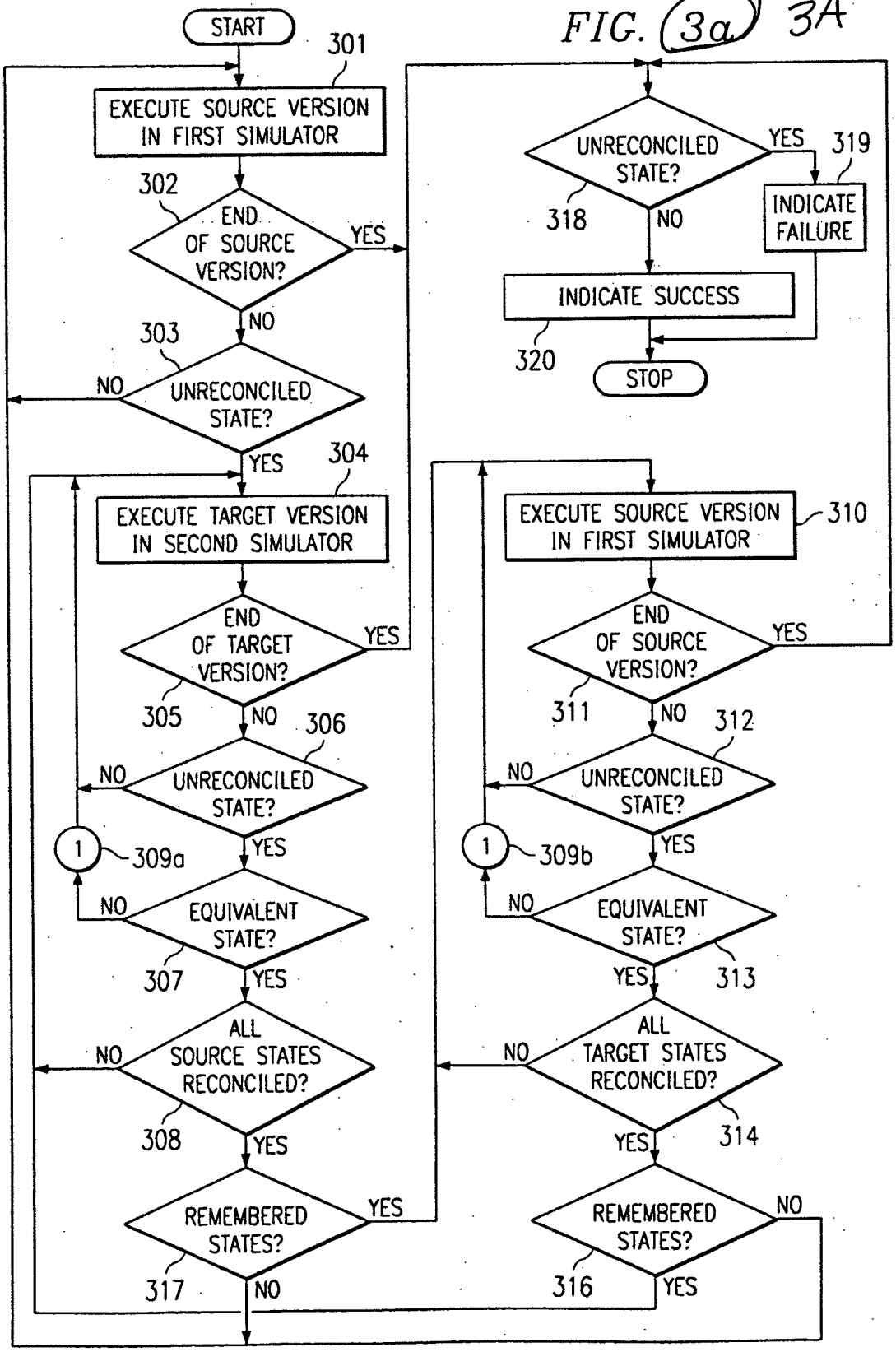
START
301
EXECUTE SOURCE VERSION IN FIRST SIMULATOR
302
END OF SOURCE VERSION?
YES
NO
303
UNRECONCILED STATE?
NO
YES
304
EXECUTE TARGET VERSION IN SECOND SIMULATOR
END OF TARGET VERSION?
YES
305
NO
306
UNRECONCILED STATE?
NO
YES
1
309a
EQUIVALENT STATE?
NO
307
YES
ALL SOURCE STATES RECONCILED?
NO
308
YES
REMEMBERED STATES?
YES
317
NO
EXECUTE SOURCE VERSION IN FIRST SIMULATOR
310
END OF SOURCE VERSION?
YES
311
NO
312
UNRECONCILED STATE?
NO
YES
1
309b
EQUIVALENT STATE?
NO
YES
313
ALL TARGET STATES RECONCILED?
NO
YES
314
REMEMBERED STATES?
NO
316
YES
UNRECONCILED STATE?
YES
319
318
NO
INDICATE FAILURE
INDICATE SUCCESS
320
STOP

FIG. 3b

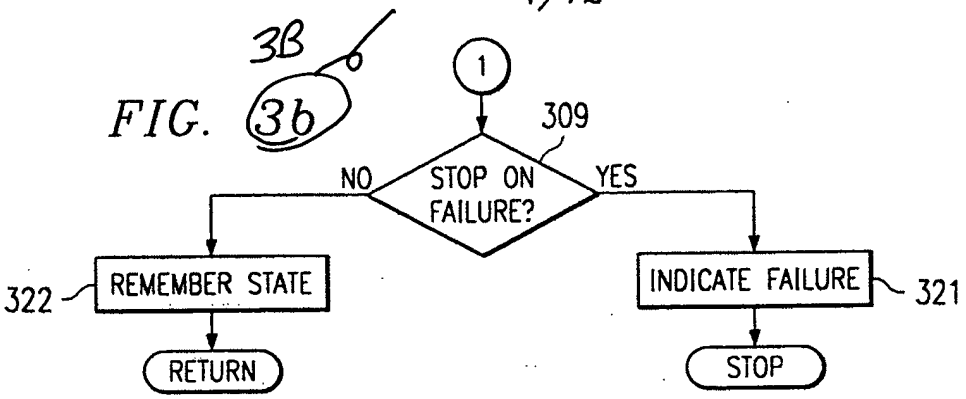

FIG. 4b

SOURCE EXECUTION	SOURCE	SOURCE STATE	TARGET EXECUTION	TARGET	TARGET STATE
	STM data1, AR3	AR3=0x800		MOV data1, AR3	EMPTY
	LD #1, A		402	MOV #1, AC0	
401	NOP			NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4c

SOURCE EXECUTION	SOURCE	SOURCE STATE	TARGET EXECUTION	TARGET	TARGET STATE
	STM data1, AR3	AR3=0x800		MOV data1, AR3	XAR3= 0x430
	LD #1, A			MOV #1, AC0	
401	NOP		402	NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

SOURCE EXECUTION (403)	SOURCE	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 A=1		MOV data1, AR3	XAR3= 0x430
	LD #1, A			MOV #1, AC0	
→ 401	NOP		→ 402	NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4d 4D

SOURCE EXECUTION (403)	SOURCE	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 A=1		MOV data1, AR3	XAR3= 0x430 AC0=1
	LD #1, A			MOV #1, AC0	
→ 401	NOP		→ 402	NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4e 4E

SOURCE EXECUTION (403)	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION (404)	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 (*AR3)=1		MOV data1, AR3	XAR3= 0x430
	LD #1, A			MOV #1, AC0	
	NOP		→	NOP	
	NOP		402	NOP	
401	STL A, *AR3+			MOV AC0<<#0, AR3+	
→	NOP			NOP	

FIG. 4f 4F

SOURCE EXECUTION (403)	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION (404)	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 (*AR3)=1		MOV data1, AR3	XAR3= 0x430 (*XAR3)=1
	LD #1, A			MOV #1, AC0	
	NOP			NOP	
	NOP			NOP	
401	STL A, *AR3+		402	MOV AC0<<#0, AR3+	
→	NOP		→	NOP	

FIG. 4g 4G

FIG. 4h 4H

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	EMPTY		MOV data1, AR3	EMPTY
	LD #1, A			MOV #1, AC0	
	NOP			NOP	
	NOP			NOP	
401 →	STL A, *AR3+		402 →	MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 5a 5A

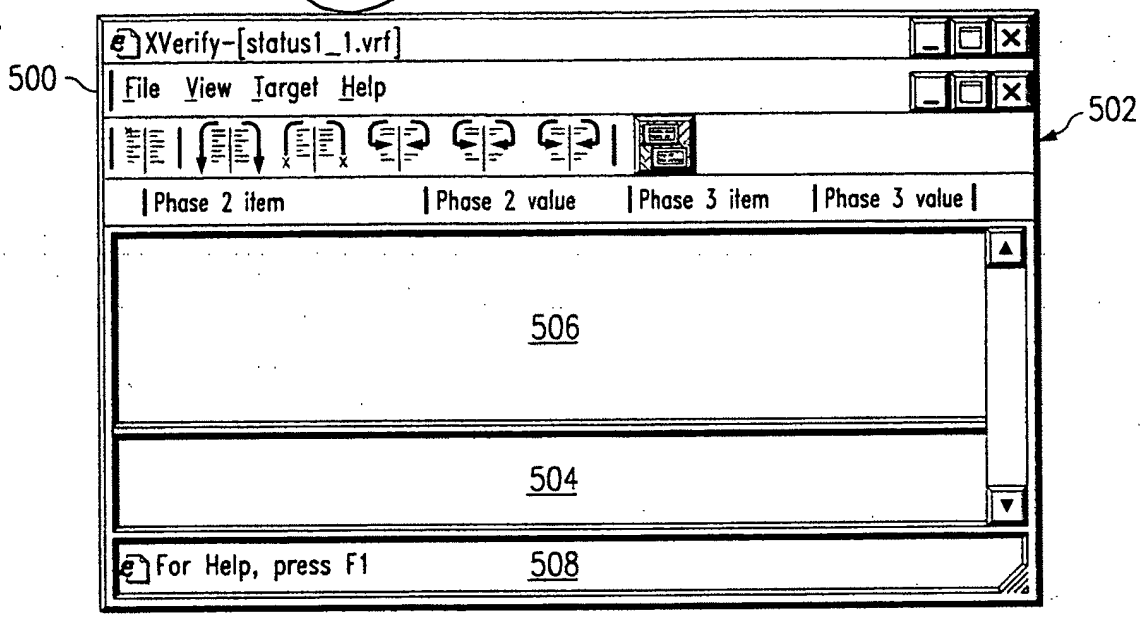

FIG. 5b 5B

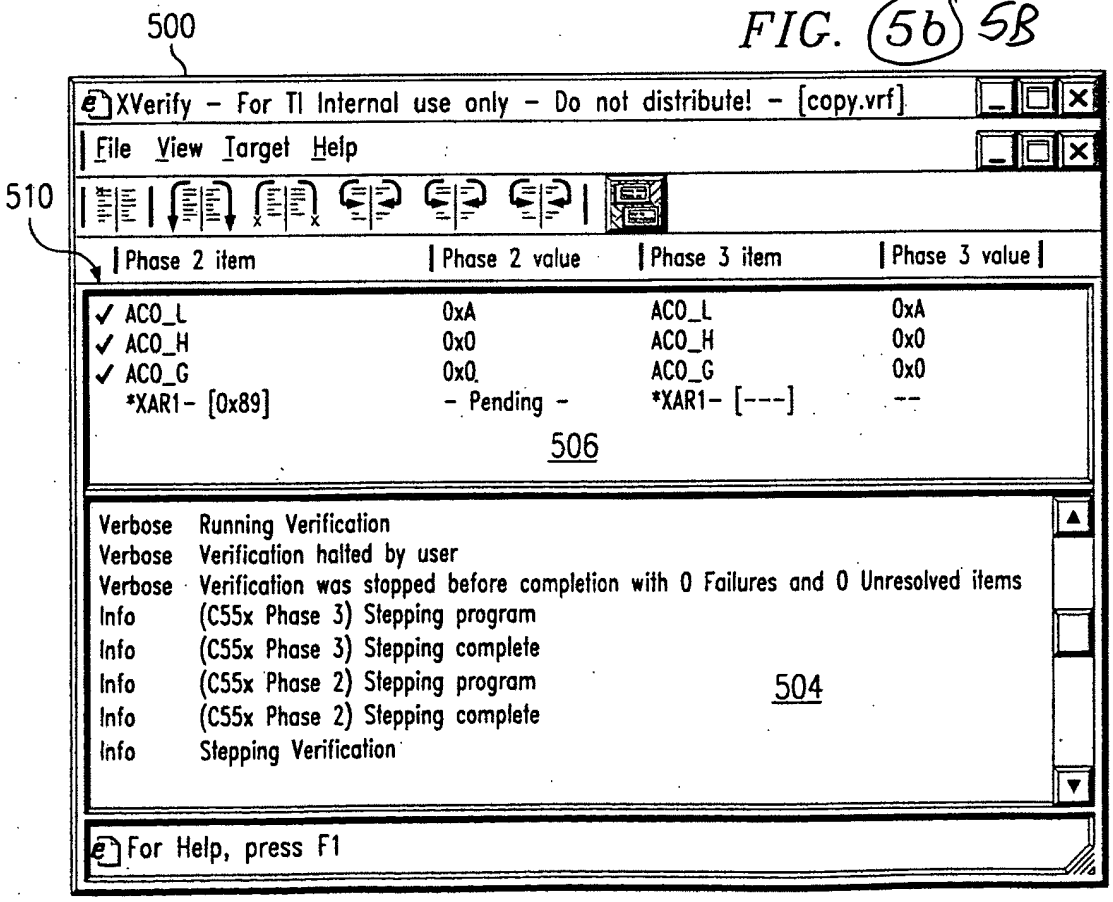

FIG. 6a 6A

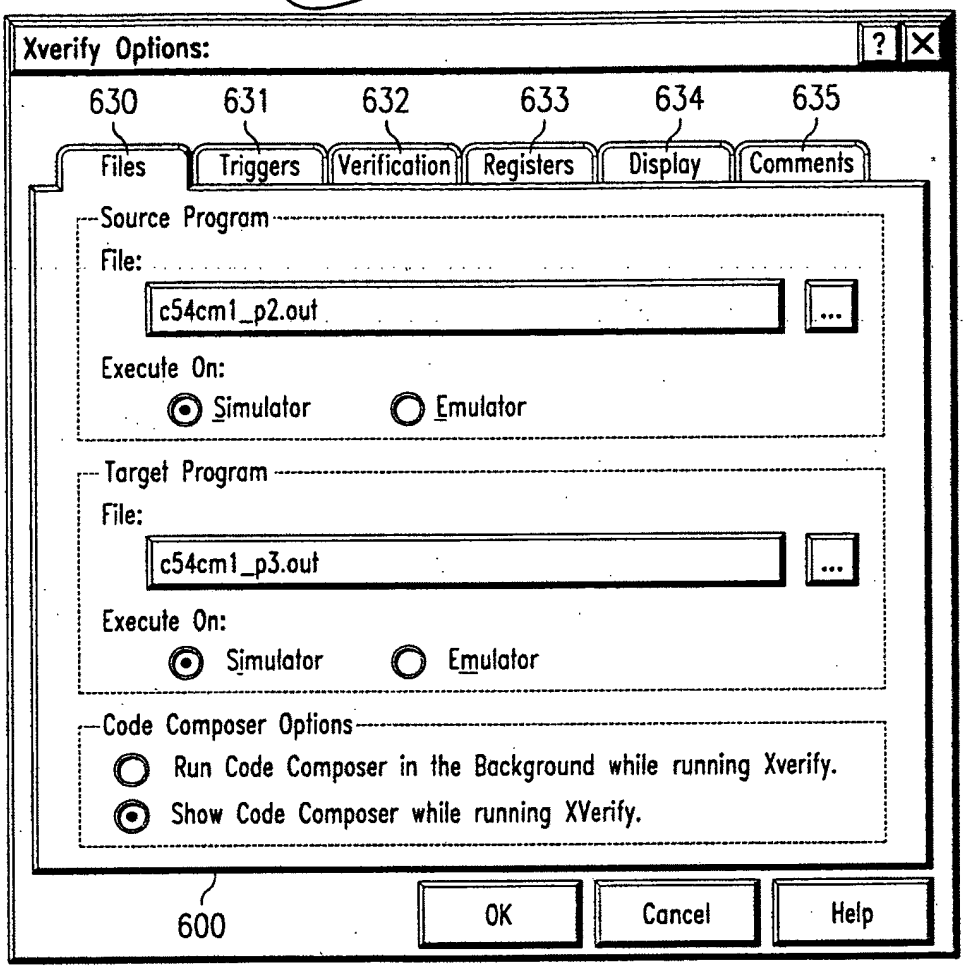

FIG. 6d 6D

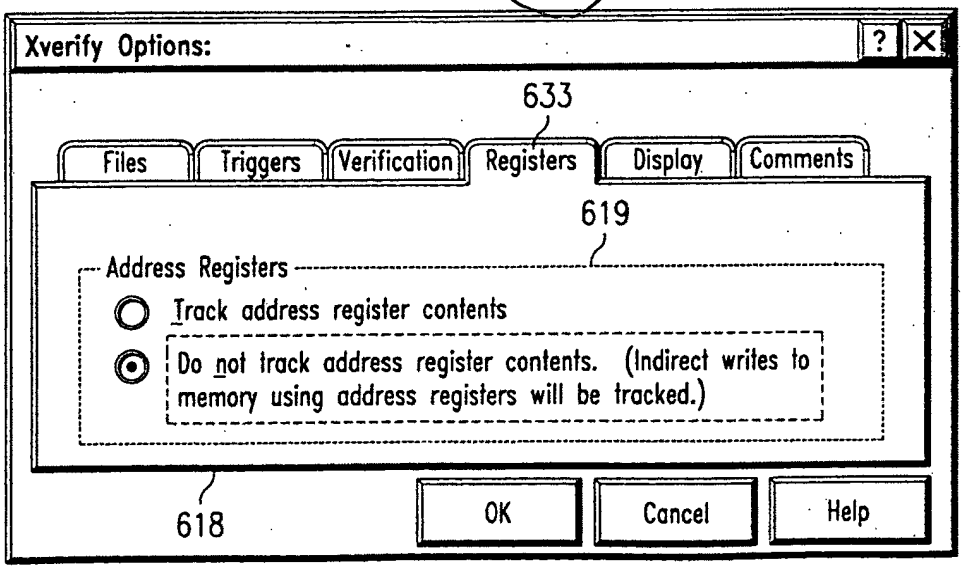

FIG. 6b 6B

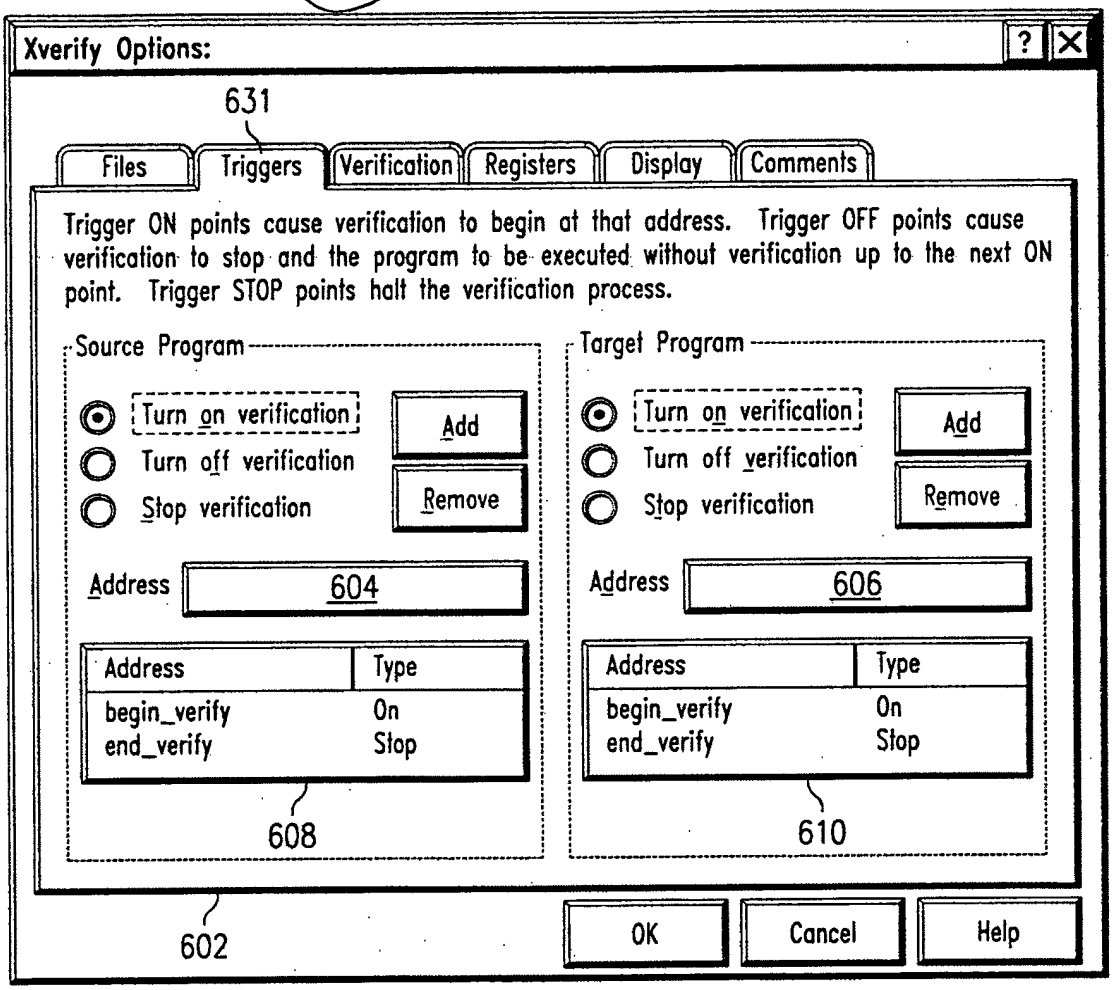

FIG. 6f 6F

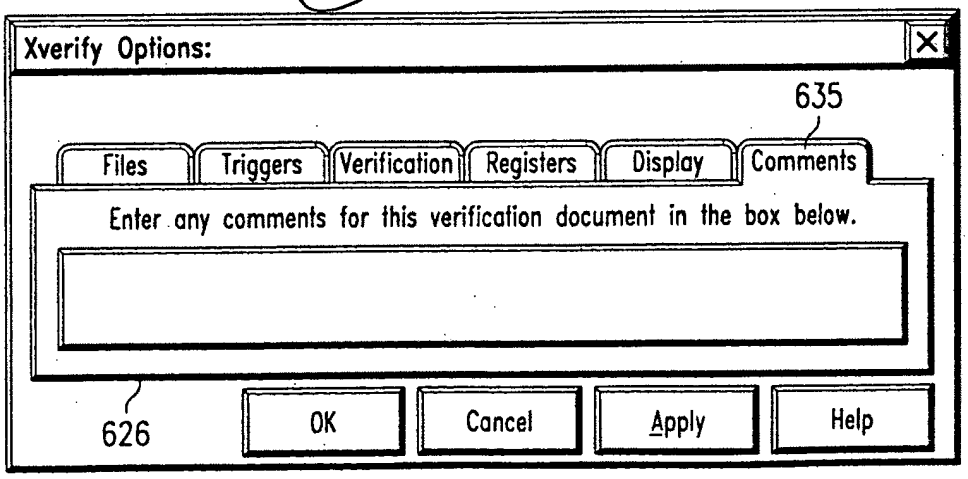

FIG. 6c 6C 11/12

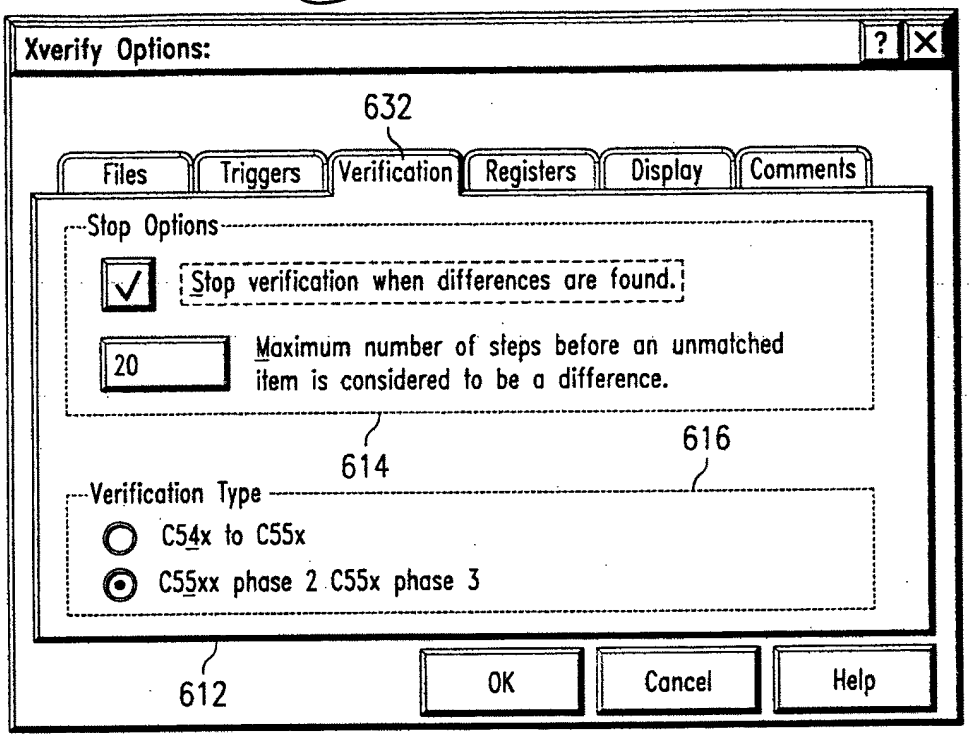

FIG. 6e 6E